a reprogramming arrangement reprogramming information in a memory arrangement of a computer, the reprogramming arrangement selecting an identifier from the information entered into an area of the memory arrangement to be erased and/or programmed, the identifier identifying a correct erasing and/or programming of the memory arrangement.

Please add the following new claims:

--29. (New) The method of claim 1 wherein the information includes data.

30. (New) The method of claim 1 wherein the information includes programs.

31. (New) The method of claim 12 wherein the information includes data.

32. (New) The method of claim 12 wherein the information includes programs. --

REMARKS

Claims 1-32 are pending. By this Response, claims 29-32 have been added. Reconsideration and allowance of the pending claims are respectfully requested.

The Examiner has refused to consider the German Patent Application Nos. 196 19 354 and 196 23 145, which are listed in the IDS submitted on March 17, 2000, on the grounds that the IDS does not include a concise explanation of the relevance of the foreign language documents. Applicants point out, however, that 37 CFR §1.98(a)(3) states that with regard to foreign language documents, the "concise explanation may be either separate from applicant's specification *or incorporated therein*." (Emphasis added). Page 1, line 8 through page 2, line 16 of the specification provides explanation of the relevance of each of these documents. Accordingly, Applicants request that the Examiner duly consider these references.

Claims 1-28 have been rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Applicants traverse this rejection and respectfully assert that the claims are enabled.

Specifically, the Examiner has indicated that the specification does not provide enabling support for the "and/or" language recited in the claims. With regard to the term "erasing and/or programming," Applicants point out that the discussion at page 4, lines 14-19 of the specification refers to three types of flash EPROMS by way of example, in which the EPROMS "differ greatly with regard to erasing and/or programming." The description provides for scenarios in which the EEPROM is only erased, only programmed, as well as erased and programmed. With regard to the term "data and/or

program," Applicants point out that the discussion at page 5, lines 13-30 of the specification indicates that vector tables, programming routines and application programs are examples of the types of information that can be erased and/or programmed in the claimed memory arrangement. For at least the foregoing reasons, claims 1-28 are enabled. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

Claims 1-28 have also been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Specifically, the Examiner has indicated that the language "and/or" fails to particularly point out and distinctly claim the subject matter to which Applicants regard as the invention. As already discussed, specific examples are provided with regard to erasing and programming, as well as data and programs. Notwithstanding, Applicants have amended the claims to more generally recite "information" as opposed to "data and/or programs." For at least the foregoing reasons, claims 1-28 are definite. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

Claims 1-6, 12-18 and 24-28 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,930,826 to Lee et al. Applicants traverse this rejection and assert that Lee does not satisfy a *prima facie* case of obviousness for the reasons stated below.

With specific regard to claims 1, 12, 24 and 27, Applicants point out that Lee fails to describe an identifier identifying a *correct* erasing and/or programming of a memory arrangement. Rather, the protection bits 81, 82, 83 of Lee are used to identify *whether* erasing, programming or reading of a memory sector 80 are permitted. The decision to permit erasing, programming or reading of the memory sector 80 of Lee is made by servicing personnel. Thus, Lee provides no relationship between a correct erasing and/or programming of memory sector 80 and the status of the protection bits 81, 82, 83. For at least the above reasons, claims 1, 12, 24 and 27 are allowable over Lee. Claims 2-6, 13-18, 25, 26 and 28 depend from claims 1, 12 or 24, so claims 2-6, 13-18, 25, 26 and 28 are also allowable over Lee. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

Claims 7-11 and 19-23 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Japan Patent Application No. 09 161 493 to Yousuke et al. ("Yousuke").

At the outset, Applicants point out that the rejected claims depend from claims 1 and 12 discussed above. While the Examiner relies on Yousuke to cure the deficiencies of Lee as applied against claims 1 and 12, Applicants point out that there is no ostensible motivation to modify Lee to include an identifier identifying a correct erasing and/or programming of a memory arrangement. Lee clearly states that status of the

protection bits can only be changed during a special protection mode (see col. 5, lines 64-65). Indeed, Lee teaches away from using the protection bits to identify a correct erasing and/or programming of the memory sector by suggesting that a series of commands be required to enter the special protection mode in order to prevent unintentional changes of the protection bits (see col. 6, lines 18-20).

With specific regard to claims 7 and 19, Applicants point out that Lee also fails to describe the *altering* of an identifier in a memory arrangement before erasing and/or programming information so that the identifier is *unidentifiable*, as the Examiner has already noted. Rather, Lee teaches the use of protection bits, which are either set or not set, and are therefore *identifiable* after alteration. Yousuke sets a write execution display flag before the write operation, and if the write operation is successful, the write execution display flag is replaced with a write end display flag. Indeed, the flags are quite similar to the bits of Lee. Thus, both flags are identifiable.

With specific regard to claims 8 and 20, Lee fails to describe an identifier being a section of a program identifier, as the Examiner has already noted. Rather, Lee teaches the use of separate protection bits, as discussed above. While the Examiner relies on Yousuke to provide a program identifier, Applicants respectfully assert that the display flags of Yousuke are not program identifiers as claimed. Indeed, Yousuke makes no mention of program identifiers.

For at least the above reasons, claims 7-11 and 19-23 are allowable over Lee and Yousuke. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

CONCLUSIONS

Applicants submit that all pending claims are in condition for allowance. Accordingly, Applicants respectfully request the Examiner issue this case at the Examiner's earliest possible convenience.

The Commissioner is hereby authorized to charge any additional fees required or credit any overpayment in connection with this correspondence to Deposit Account 11-0600.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Dated: 7/31/02

By: for Richard L. Mayer (by S. Lee R. No. 36,197)

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APPENDIX A

Version with markings to show changes made

IN THE CLAIMS:

Please substitute the amended claims below for the pending claims with the same claim numbers. Insertion is shown by underlining and deletion is shown by strikethrough.

Please amend claims 1, 6, 8, 12, 14, 16 18, 20, 24 and 27 as follows:

1. (Amended Twice) A method of erasing and/or programming information ~~data and/or programs~~ in a memory arrangement of a computer, comprising the steps of:

providing an identifier into an area of the memory arrangement that is to be erased and/or programmed, the identifier identifying a correct erasing and/or programming of the memory arrangement; and

altering the identifier in the memory arrangement before erasing and/or programming the information ~~data and/or the programs~~.

6. (Amended) The method according to claim 1, wherein the identifier is ~~at least one of~~ a component of the information ~~data and a component of the programs~~.

8. (Amended) The method according to claim 1, wherein the identifier is a section of a program identifier which identifies the respective information ~~data and/or the programs~~.

12. (Amended) A method of reprogramming information ~~data and/or programs~~ in a memory arrangement of a computer, comprising the step of:

selecting an identifier from the information ~~data and/or the programs~~ entered into an area of the memory to be erased and/or programmed, the identifier identifying a correct erasing and/or programming of the memory arrangement.

14. (Amended) The method according to claim 12, further comprising the step of:

selecting the identifier from the information ~~data and/or the programs~~ entered into a further area of the memory arrangement, the further area being erased and/or programmed only after erasing and/or programming of the area.

16. (Amended) The method according to claim 12, further comprising the step of:

altering the selected identifier in the memory arrangement before erasing and/or programming the information ~~data and/or the programs~~.

18. (Amended) The method according to claim 12, further comprising the step of:

selecting the identifier as at least one section of a predetermined length of the information ~~data and/or the programs~~ entered into the memory arrangement.

20. (Amended) The method according to claim 12, wherein the identifier is a section of a program identifier which identifies the information ~~data and/or the programs~~.

24. (Amended) A device for erasing and/or programming information ~~data and/or programs~~ in a memory arrangement of a computer, comprising:

a programming arrangement entering an identifier into an area of the memory arrangement to be erased and/or programmed, the identifier identifying a correct erasing and/or programming of the memory arrangement, the programming arrangement altering the identifier in the memory arrangement before erasing and/or programming the information ~~data and/or the programs~~.

27. (Amended) A device, comprising:

a reprogramming arrangement reprogramming information ~~data and/or programs~~ in a memory arrangement of a computer, the reprogramming arrangement selecting an identifier from the information ~~data and/or the programs~~ entered into an area of the memory arrangement to be erased and/or programmed, the identifier identifying a correct erasing and/or programming of the memory arrangement.